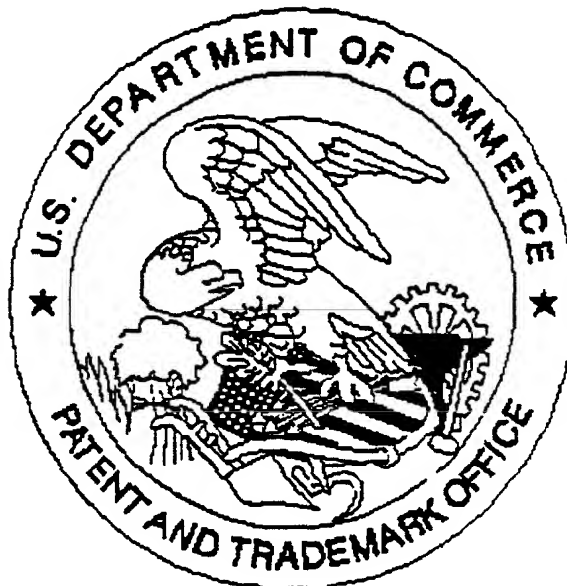


# REFERENCE NUMERALS

	first TAP <b>12</b> , called Master TAP	[ 5 ]
	eTAP1 <b>14</b>	[ 5 ]
5	eTAP2 <b>16</b>	[ 5 ]
	processor cores <b>18</b> and <b>20</b>	[ 7 ]
	first group <b>22</b> of TAPs	[ 7 ]
	second group <b>24</b>	[ 7 ]
	shift register <b>30</b>	[ 8 ]
10	update register <b>32</b>	[ 9 ]
	multiplexer <b>34</b>	[ 9 ]
	shift register <b>36</b>	[ 9 ]
	an associated update register <b>38</b>	[ 9 ]
	multiplexer <b>40</b>	[ 10 ]
15	TDO multiplexer <b>42</b>	[ 11 ]
	TMS gating circuit <b>50</b>	[ 11 ]
	RESET gating circuit <b>52</b>	[ 12 ]
	Master TAP <b>100</b>	[ 12 ]
	embedded TAPS <b>102</b> , <b>104</b> and <b>106</b>	[ 12 ]
20	three TAP groups <b>110</b> , <b>112</b> and <b>114</b>	[ 12 ]
	instruction register <b>116</b>	[ 13 ]
	instruction registers <b>118</b> and <b>120</b>	[ 13 ]
	group TDI node <b>122</b>	[ 13 ]
	group TDO node <b>124</b>	[ 13 ]
25	instruction register <b>125</b> of the Master TAP	[ 13 ]
	TDI input <b>126</b>	[ 13 ]
	TDI multiplexers <b>132</b> and <b>134</b> associated with embedded TAP groups <b>112</b> and <b>114</b> , respectively	[ 14 ]
	a data register, such as shown by reference numeral <b>136</b> in FIG. 3	[ 16 ]
30	circuit <b>60</b>	[ 17 ]
	Master TAP <b>62</b>	[ 17 ]
	test data register <b>64</b>	[ 17 ]
	embedded TAP <b>66</b>	[ 17 ]
	multiplexer <b>70</b>	[ 17 ]
35	a multiplexer <b>72</b>	[ 17 ]

FIG. 3

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